REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on May 8, 2003, and the references cited therewith.

Claim 1 is amended, no claims are canceled or added; as a result, claims 1-30 are now pending in this application.

Formal Drawings

Applicant respectfully submits formal drawings with this response.

The Kwak et al. reference

Applicant does not admit that the Kwak et al. reference is prior art, and reserves the right to swear behind the Kwak et al. reference at a later date. Nevertheless, Applicant respectfully submits that the claims are distinguishable over Kwak et al. reference for the reasons presented below.

§102 Rejection of the Claims

Claims 1, 7-9, 21, 22 and 27 were rejected under 35 USC § 102(e) as being anticipated by Kwak et al. (U.S. 2002/0039044).

Independent claim 21 recites a current reference comprising, among other elements, a control loop circuit responsive to "a current equal to the generated current", and the control loop circuit coupled "to influence the generated current".

Kwak et al. does not disclose several elements of claim 21.

For example, Kwak et al. does not disclose a control loop circuit responsive to a "current". Kwak et al. discloses, in FIG. 3, a reference voltage with a voltage supply circuit (120) having a *voltage* Vrefb, not a current. Notwithstanding that Kwak et al. does not disclose a "current", Kwak et al. does not disclose the current being "equal to the generated current".

Additionally, Kwak et al. does not disclose a control loop circuit coupled "to influence the generated current". Kwak et al., disclose a voltage supply circuit 120 is to force an active resistance device (transistor Q12) to operate in a linear region. Kwak et al. does not disclose that voltage supply circuit 120 influences a current such as the generated current as recited in claim 21.

Since Kwak et al. does not disclose all of the elements recited in claim 21, claim 21 is not anticipated by Kwak et al. Applicant requests that the rejection of claim 21 be reconsidered and withdrawn and that claim 21 be allowed.

Claim 22 depends from claim 21. Thus, claim 22 is also not anticipated by Kwak et al. for the reasons presented above regarding claim 21. Applicant requests that the rejection of claim 22 be reconsidered and withdrawn and that claim 22 be allowed.

Independent claim 1 is amended to include elements similar to the elements of claim 21. Thus, claim 1 is also not anticipated by Kwak et al. because Kwak et al. does not disclose all of the elements of the amended claim 1 as explained above regarding claim 21. Applicant requests that the rejection of claim 1 be reconsidered and withdrawn and that claim 1 be allowed.

Claims 7-9 depend from claim 1. Thus, claims 7-9 are also not anticipated by Kwak et al. for the reasons presented above regarding claim 1. Applicant requests that the rejection of claims 7-9 be reconsidered and withdrawn and that claims 7-9 be allowed.

Independent claim 27 recites, among other elements, a control loop circuit comprising a "variable impedance" output driver. Kwak et al. disclose, in FIG. 3, a voltage generating circuit (120). The Office Action treats voltage generating circuit 120 as the control loop circuit of claim 1. However, the Office Action did not indicate which element of voltage generating circuit 120 of Kwak et al. comprises a "variable impedance" output driver. Thus, Applicant is unable to identify in Kwak et al. which element is a "variable impedance" output driver. However, to expedite the prosecution of this application, Applicant made an assumption that each element or a combination of the elements of voltage generating circuit 120 may represent the "variable impedance" output driver of claim 1.

With assumption above, Applicant respectfully points out that each element or a combination of the elements (transistors Q13, Q14, Q15, and Q16) of voltage generating circuit 120 is not a "variable impedance" output driver. For example, transistor Q13 is not a "variable impedance" output driver because transistor Q13 operates in saturation region as transistors Q8 and Q9 do. A transistor operating in saturation region such as transistor Q13 has fixed impedance. Thus, transistor Q13 is not a "variable impedance" output driver. As another example, each of the transistors Q14 through Q16 is connected as a diode. A diode-connected transistor has fixed impedance. Thus, transistor Q14, Q15, or Q16 is not a "variable impedance"

output driver. Although the number of transistors Q14, Q15, and Q16 may be varied as indicated by Kwak et al., a combination of a number of diode-connected transistors themselves would not produce a "variable impedance" output driver. Thus, the combination of three diode-connected transistors Q14, Q15, Q16 (or other numbers, e.g., four or five diode-connected transistors) is not a "variable impedance" output driver.

Since the Office Action did not indicate which element in Kwak et al. is relied upon as a "variable impedance" output driver, Kwak et al. does not disclose a control loop circuit comprising a "variable impedance" output driver. Thus, the Office Action failed to show that claim 27 is anticipated by Kwak et al. Accordingly, Applicant requests that the rejection of claim 27 be reconsidered and withdrawn and that claim 27 be allowed.

§103 Rejection of the Claims

Claims 2-5, 23 and 26 were rejected under 35 USC § 103(a) as being unpatentable over Kwak et al. in view of Kwan (U.S. 5,949,279).

Dependent claims 2-5 depend from amended claim 1. As presented in the explanation related to the §102 rejection above, Kwak et al. does not disclose all of the elements of claim 1. For example, Kwak et al. does not disclose a "current" and the current being "equal to the generated current". Since Kwak et al. does not disclose all of the elements of claim 1, Kwak et al. also does not disclose all of the elements of claims 2-5 because claims 2-5 incorporate the elements of claim 1 together with additional elements. The proposed combination of Kwak et al. and Kwan also does not disclose all of the elements of claims 2-5. Thus, claims 2-5 are patentable over Kwak et al. and Kwan. Applicant requests that the rejection of claims 2-5 be reconsidered and withdrawn and that claims 2-5 be allowed.

Claims 23 and 26 depend from claim 21. As presented in the explanation related to the §102 rejection above, Kwak et al. does not disclose all of the elements of claim 21. The proposed combination of Kwak et al. and Kwan also does not disclose all of the elements of claims 23 and 26. Thus, claims 23 and 26 are patentable over Kwak et al. and Kwan. Applicant requests that the rejection of claims 23 and 26 be reconsidered and withdrawn and that claims 23 and 26 be allowed.

Claims 6, 24, 25 and 28-30 were rejected under 35 USC § 103(a) as being unpatentable over Kwak et al. in view of Kwan and in view of Burger, Jr. et al. (U.S. 6,275,090).

Claim 6

Claim 6 recites, among other elements:

> a variable resistor coupled between the first and second biasing terminals of the control transistor and coupled to the current mirror to receive the second current; and
>
> a control loop circuit to influence the variable resistor, wherein the variable resistor comprises a plurality of resistive devices in parallel, each of the plurality of resistive devices having a control input node to enable the resistive device, wherein the control loop circuit comprises:
>
> a comparator to compare two voltages, the comparator having an output node; and
>
> a state machine coupled to the output node of the comparator, the state machine having output nodes coupled to the control input nodes of the plurality of resistive devices.

Kwak et al. does not disclose or suggest several elements recited in claim 6 such as a variable resistor comprising a plurality of resistive devices in parallel, a comparator to compare two voltages, the comparator having an output node, and a state machine coupled to the output node of the comparator, the state machine having output nodes coupled to the control input nodes of the plurality of resistive devices.

The Office Action fails to show evidence of a reason to combine Kwan with Kwak et al. It also fails to show a reason to combine Burger, Jr. et al. with the combination of Kwak et al. and Kwan to achieve the claimed invention as claimed in claim 6.

Kwan discloses a plurality of resistors connected in parallel. The values of the resistors are selected by digital signals on lines 102. Kwak et al. teaches an active resistance device (transistor Q12) controlled by signal Vrefb to force transistor Q12 to operate in linear region. Kwak et al. does not teach or suggest anything about replacing a linear operated transistor with parallel resistors. Nonetheless, replacing transistor Q12 of Kwak et al. with the parallel resistors of Kwan would destroy the operation of the circuit of Kwak et al. because Vref is an analog signal unsuitable for controlling a plurality of parallel resistors to achieve the same function as that of transistor Q12. Thus, there is no motivation or reason to combine Kwak et al. and Kwan.

Applicant traverses the contention that it would have been obvious to employ the teaching of Burger, Jr. et al. to realize the "modified" circuit of Kwak et al. The modifications to the circuit of Kwak et al., as proposed in the Office Action, are the combination of Kwak et al. and Kwan in which the parallel resistors of Kwan replace transistor Q12 of Kwak et al. Applicant respectfully submits that the Office Action fails to show a reason or motivation to combine Burger, Jr. et al. with the combination of Kwak et al. and Kwan because Burger, Jr. et al., Kwak et al., and Kwan disclose circuits for different purposes.

Kwak et al. discloses a circuit (120) for controlling a gate voltage of a transistor (Q12) to force the transistor to operate in the linear region. Burger, Jr. et al. discloses a comparator and a state machine for trimming values of a plurality of resistors connected in series. Kwak et al. does not disclose or suggest anything about trimming values of a plurality of resistors connected in series. The Office Action fails to show a motivation or reason to combine Burger, Jr. et al. with the "modified" circuit of Kwak et al., or the combination of Kwak et al. and Kwan. Even if Burger, Jr. et al. were combined with Kwak et al. and Kwan as proposed in the Office Action, such a combination would not be possible because Burger, Jr. et al. disclose a state machine for controlling to a plurality of resistors in which the resistors are connected in series. In contrast, the resistors of Kwan are connected in parallel, not series.

The reasons presented above demonstrate that the Office Action fails to state a prima facie showing of obviousness because the Office Action provides no evidence of a reason to combine Kwak et al., Kwan, and Burger, Jr. et al.

Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

Moreover, the claimed invention as claimed in claim 6 was not considered as a whole. In determining the differences between the prior art and the claim, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698

(Fed. Cir. 1983); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985); MPEP § 2141.02.

Based on all of the reasons presented above, the Office Action fails to show that claim 6 is obvious over Kwak et al. in view of Kwan and in view of Burger, Jr. et al. Applicant requests that the rejection of claim 6 be reconsidered and withdrawn and that claim 6 be allowed.

Claims 24 and 25

Claims 24 and 25 depend from claim 21. As presented in the explanation related to the §102 rejection above, Kwak et al. does not disclose all of the elements of claim 21. For example, Kwak et al. does not disclose a "current" and the current being "equal to the generated current". Since Kwak et al. does not disclose all of the elements of claim 21, Kwak et al. also does not disclose all of the elements of claims 24 and 25 because claims 24 and 25 incorporate the elements of claim 21. The proposed combination of Kwak et al., Kwan, and Burger, Jr. et al. also does not disclose all of the elements of claims 24 and 25. Thus, claims 24 and 25 are patentable over Kwak et al., Kwan, and Burger, Jr. et al. Applicant requests that the rejection of claims 24 and 25 be reconsidered and withdrawn and that claims 24 and 25 be allowed.

Claims 28-30

Claims 28-30 depend from claim 27. As presented in the explanation related to the §102 rejection above, Kwak et al. does not disclose all of the elements of claim 27. For example, Kwak et al. does not disclose a "variable impedance" output driver. Since Kwak et al. does not disclose all of the elements of claim 27, Kwak et al. also does not disclose all of the elements of claims 28-30 because claims 28-30 recite the elements of claim 27. The proposed combination of Kwak et al., Kwan, and Burger, Jr. et al. also does not disclose all of the elements of claims 28-30. Thus, claims 28-30 are patentable over Kwak et al., Kwan, and Burger, Jr. et al. Applicant requests that the rejection of claims 28-30 be reconsidered and withdrawn and that claims 28-30 be allowed.

Claims 10-20 were rejected under 35 USC § 103(a) as being unpatentable over Kwak et al. in view of Kwan, Burger, Jr. et al. and Perque et al. (U.S. 2002/0014914).

Independent claim 10 recites an integrated circuit comprising, among other elements, a first current reference, a first current mirror, a second current reference, a second current mirror, a first variable resistor, a second variable resistor, and control loop coupled to an output node of the second current reference to influence the first and second variable resistors.

The proposed combination of Kwak et al., Kwan, Burger, Jr. et al., and Perque et al. does not disclose all of the elements including "a first current mirror", "a second current mirror", "a first variable resistor", "a second variable resistor", and "control loop coupled to an output node of the second current reference to influence the first and second variable resistors".

Since the proposed combination of Kwak et al., Kwan, Burger, Jr. et al., and Perque et al. does not disclose all of the elements recited in claim 10, claim 10 is not anticipated by the proposed combination of Kwak et al., Kwan, Burger, Jr. et al., and Perque et al. Applicant requests that the rejection of claim 10 be reconsidered and withdrawn and that claim 10 be allowed.

Claims 11-20 depend from claim 10. Thus, claims 11-20 are also patentable over the proposed combination of Kwak et al., Kwan, Burger, Jr. et al., and Perque et al. for the reasons presented above, plus the elements in claims 11-20. Applicant requests that the rejection of claims 11-20 be reconsidered and withdrawn and that claims 11-20 be allowed.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative (612-373-6969) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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